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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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ZAGORIN O'BRIEN GRAHAM LLP (004)
7600B NORTH CAPITAL OF TEXAS HIGHWAY
SUITE 350
AUSTIN, TX 78731-1191

EXAMINER	
DONAGHUE, LARRY D	
ART UNIT	PAPER NUMBER
2154	

DATE MAILED: 05/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/779,944	JOY ET AL.	
	Examiner	Art Unit	
	Larry D. Donaghue	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-19 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-19 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 02/17/2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date attached.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-19 are presented for examinations.

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-19 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-2 of U.S. Patent No. 6,507,862. Although the conflicting claims are not identical, they are not patentably distinct from each other.

4. 6,507,862 corresponded to claims 1 and 11 of the instant application as follows:

Claim 1, A computing system comprising: at least part of a memory hierarchy (Claim 2, lines 1-6); and a processor that stores plural execution contexts in a pipeline thereof , the processor performing a context switch between a first one and a second one of the execution contexts by freezing the first execution context in the pipeline (claim 1, lines 2-10) and resuming execution using previously frozen state corresponding to the second execution context, the context switching performed without draining the first execution context from the pipeline (claim 1, lines 11-13).

Claim 11, A method of operating a processor, the method comprising: executing plural execution contexts in a pipeline of the processor (claim 1, lines 2-7); and performing a context switch between a first one and a second one of the execution contexts by freezing the first execution context in the pipeline (claim 1, lines 8-10) and resuming execution using previously frozen state corresponding to the second execution context (claim 1 lines 11-16), the context switching performed without draining the first execution context from the pipeline (claim 1, lines 11-13).

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1,5,7-11 and 13-18 rejected under 35 U.S.C. 102(b) as being clearly anticipated by Okin (5,361,337).

As to claim 1, Okin taught a computing system comprising: at least part of a memory hierarchy (col. 1, lines 17-46); and a processor that stores plural execution contexts in a pipeline thereof, the processor performing a context switch between a first one and a second one of the execution contexts by freezing the first execution context in the pipeline and resuming execution using previously frozen state corresponding to the second execution context, the context switching performed without draining the first execution context from the pipeline (col. 4, lines 1-26).

As to claim 5, Okin taught context selectable storage distributed throughout the pipeline, the context selectable storage coupled into the pipeline to represent intermediate pipeline states for at least two concurrently executing execution contexts (figure 4, 30,32,38; 30', 32',38'; 30", 32", 38").

As to claim 7, Okin taught a context-selectable register file coupled to the pipeline to represent architectural states for at least two concurrently executing execution contexts.

As to claim 8, Okin taught wherein the context switch is performed without saving and restoring the execution contexts to and from the register file (col. 4, lines 1-26).

As to claim 9, Okin taught wherein the memory hierarchy includes cache defined on die with the processor(col. 1, lines (col. 1, lines 17-46) .

As to claim 10, Okin taught wherein the memory hierarchy includes memory coupled to the processor via at least one bus (col. 1, lines 17-46).

As to claim 11, Okin taught executing plural execution contexts in a pipeline of the processor; and performing a context switch between a first one and a second one of the execution contexts by freezing the first execution context in the pipeline and resuming execution using previously frozen state corresponding to the second execution context, the context switching performed without draining the first execution context from the pipeline (col. 4, lines 1-26).

As to claim 13, Okin taught , further comprising: performing the context switch without saving and restoring the execution contexts to and from a register file (col. 4, lines 1-26).

As to claim 14, Okin taught maintaining a context-selectable register file coupled to the pipeline to represent architectural states for at least two concurrently executing execution contexts (col. 1-26, 32,32', 32").

As to claim 15, Okin taught at least one pipeline, including storage distributed throughout the pipeline for at least two concurrently executing execution contexts(figure 4, 30,32,38; 30', 32',38'; 30", 32", 38"), the processor supporting a context switch between a first one and a second one of the execution contexts by freezing the first

execution context in the pipeline and resuming execution using previously frozen state corresponding to the second execution context, the context switching performable without draining the first execution context from the pipeline; and a context-selectable register file coupled to the pipeline to represent architectural states for at least the two concurrently executing execution contexts (col. 4, lines 1-26).

As to claim 16, Okin taught simultaneously representing throughout a processor pipeline, state information corresponding to plural active execution contexts (figure 4, 30,32,38; 30', 32',38'; 30", 32", 38"); and switching between a first one and a second one of the active execution contexts by freezing the first execution context in the pipeline and resuming execution using previously frozen state corresponding to the second execution context, the switching performed without draining the first execution context from the pipeline (col. 4, lines 1-26).

As to claim 17, Okin taught a processor coupled to at least part of a memory hierarchy (col. 1, lines 17-46) ; and means defined in the processor for storing plural execution contexts in a pipeline thereof, the processor performing a context switch between a first one and a second one of the execution contexts by freezing the first execution context in the pipeline and resuming execution using previously frozen state corresponding to the second execution context, the context switching performed without draining the first execution context from the pipeline.

As to claim 18, Okin taught making a processor integrated circuit product, the method comprising: defining a pipelined processor; and fabricating the pipelined processor as an integrated circuit with in-pipeline storage for plural execution contexts thereof, the in-pipeline storage allowing a context switch between a first one and a second one of the execution contexts by freezing the first execution context in the pipeline and resuming execution using previously frozen state corresponding to the second execution context, the context switching performable in the fabricated pipelined processor without draining the first execution context from the pipeline (col. 4, lines 1-26) .

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okin (5,361,337) as applied to claims 1,5,7-11 and 13-18 above, and further in view of Dao et al. (6,148,395).

Okin did not expressly teach the use of a second pipeline Dao et al. taught the use of a second pipeline and the resulting improvement in throughput (col. 1); it would have been obvious to one of ordinary skill in the art to combine hese references for the benefit expressly detailed in Dao et al.

9. Claims 3-4 and 12 rejected under 35 U.S.C. 103(a) as being unpatentable over Okin (5,361,337) as applied to claims 1,5,7-11 and 13-18 above, and further in view of Official Notice.

10. As to claims 3-4, Executing a single multi-threaded application and separate context for two distinct programs is well known in the art, applying these to circuitry which will enhance their throughput would be obvious to one of ordinary skill in the art.

11. As to claim 12, in is conventional for exceptions to change context, applying this to circuitry which will enhance it's throughput would be obvious to one of ordinary skill in the art.

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following references are directed to Multithreaded processing

Amamiya et al. Datarol: A Parallel Machine Architecture for Fine-Grain Multithreading,

Braford PUMP: A New Architecture for Multithreaded Processor

The following reference discloses multi-pipeline processor

Grochowski et al. 5,442,756

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Larry D. Donaghue whose telephone number is 571-272-3962. The examiner can normally be reached on M-F 8:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Follansbee can be reached on 571-272-3964. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LARRY D. DONAGHUE
PRIMARY EXAMINER